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# Deformable Mirror Surface Control Techniques

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**A corrector mirror assembly within an optical train provides corrections to maximize energy concentration on a distant target, despite phase perturbations due to air medium turbulence. Phase correction is by mirror surface deformation provided by piezoelectric actuators and a companion, unique, solid-state, electronic amplifier. Desired actuation bandpass requirements are 1 kHz. This paper describes the overall actuation control with emphasis on the actuator and drive amplifier analysis, design, and simulation. Hardware examples are briefly presented.**

## Introduction

**A** CORRECTOR (Fig. 1) mirror within an optical train serves to control overall optical focus on a distant target.<sup>1</sup> For the intended application, primary focus error sources are from atmospheric turbulence in the beam transmission path. These are compensated for by corrective mirror surface deformation provided by 52 longitudinally acting piezoelectric actuators spaced about 3 cm apart.

Assume that, through some sensor hardware, the desired correcting mirror surface topography is known. This paper provides the actuation system algorithm and discusses the special hardware required to cause the actual mirror surface to assume the desired topography. Special hardware discussed are piezoelectric actuators and a companion, unique, solid-state, electronic drive amplifier. (The actuator algorithm and amplifier design data herein are from Ref. 2.)

Actuation requirements are a longitudinal stroke at the mirror surface of  $\pm 10 \mu\text{m}$  at low frequency, dropping to  $\pm 1 \mu\text{m}$  at 1 kHz. The mirror surface is expected to assume a "dimpled" surface pattern with at least  $2 \mu\text{m}$  difference in stroke between adjacent actuators. With respect to the 1 kHz bandpass requirement, the overall design (Fig. 1) suggests high mirror surface stiffness gained by a rugged, deep beam design of the backup structure and mirror faceplate support by the actuators, which are also quite stiff longitudinally.

A corrector mirror assembly and a brassboard amplifier model have been built and delivered.<sup>1,3</sup>

## Piezoelectric Actuator Control Loop

Figure 2 illustrates the sequence causing the output mirror surface topography to be equal to that of the input. The actuator algorithm is a divider network which compensates for variable mirror surface compliance local to each actuator. Equal gain power amplifiers for each actuator are used. Their output voltage causes an actuator output force and extension. The extension of the actuator is equal to that of the local mirror surface.

Knowledge of the piezoelectric actuator static relation between input voltage and output force and extension is prerequisite to developing the actuator algorithm and drive amplifier requirements. This relationship is summarily

presented in this paper; a more extensive treatment, including dynamic properties, can be found in Ref. 4. The actuator algorithm, example hardware, and the drive amplifier are then discussed.

## Actuator Model

Figure 3 shows a longitudinal acting piezoelectric actuator consisting of  $n$  stacked wafers which are electrically in parallel and mechanically in series. Application of a terminal voltage  $V$  causes each wafer to extend a nominal equal length. The total extension  $\delta$  is of course the sum of that from each wafer. The quantity  $K_a$  is the total actuator end-to-end stiffness constant including the disks, end fittings, electrode surfaces, etc. The quantity  $d_{33}$  is wafer material dependent and is the free extension ( $F_c = 0$ ) per input volt regardless of wafer thickness or diameter. As shown in Fig. 3, the total end force on the actuator is divided into two parts, one due to the electrical input (blocked force  $F_v$ ) and the other due to stack mechanical stiffness (compliance force  $F_c$ ).

This division is pertinent to later algorithm development where it is stated that when the structural model is for a complete actuator-faceplate-backplate assembly such as that of Fig. 1, the blocked or electrically induced forces, applied at both ends of the actuators, are the external forces applied to the assembly. The actuator compliance forces are internal to the assembly.

The resultant static or low frequency load-stroke relationship, also shown in Fig. 3, applies only when the drive voltage is below the actuator resonant frequency.

The actuator input electrical impedance is essentially capacitive. For the parallel-plate enclosed dielectric configuration used, the capacitance is given by the well-known relation  $\epsilon_0 \epsilon_r An/t$  with  $\epsilon_0$  (vacuum dielectric constant) =  $8.85 \text{ pico C}^2/\text{N-m}^2$ ; where  $\epsilon_r$  is the relative dielectric constant,  $A$  the wafer area,  $n$  the number of wafers, and  $t$  the wafer thickness.

Convenient input actuator specifications are the maximum free extension and required stiffness together with actuator total length. With maximum amplifier output voltage known and dielectric material selected, the number of wafers needed for extension is determined. In this respect, *high* amplifier output voltage is desirable because it proportionately reduces the number of wafers required together with the required electrode surfaces, wiring, etc. The required total length of the actuator yields wafer thickness and the diameter is set by the stiffness requirement. The design procedure is normally iterative, as details such as electrode thickness and end-fitting stiffness complicate the procedure.

Figure 4 shows an assembly drawing and photograph of a typical piezoelectric-actuator. The assembly consists of 30 active stacked wafers, end insulators, and attachment fittings.

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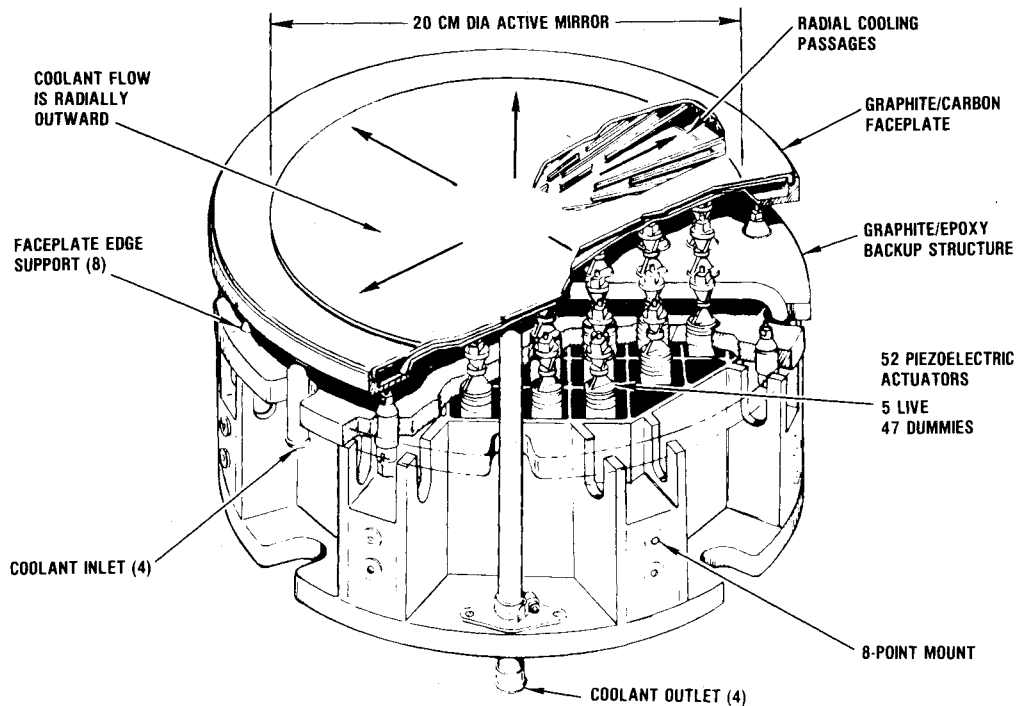


Fig. 1 Corrector mirror assembly.

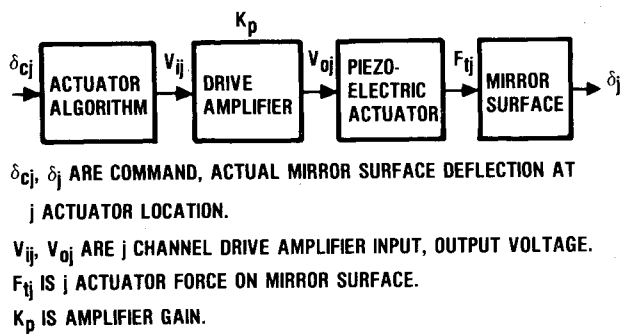


Fig. 2 Overall piezoelectric actuator model.

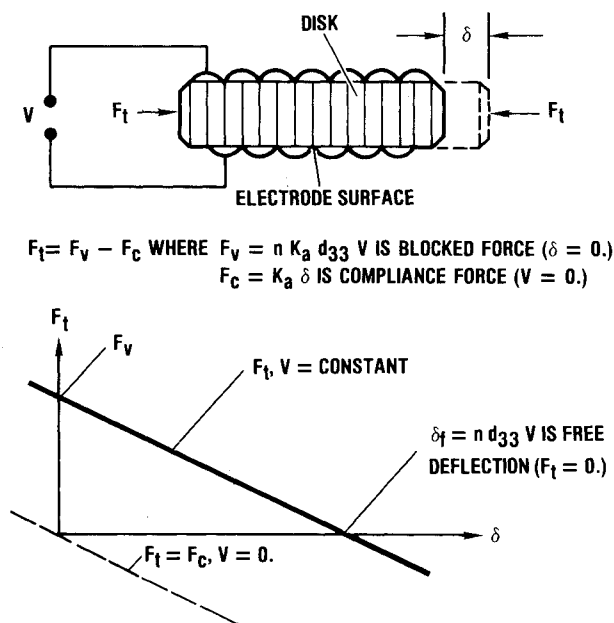


Fig. 3 Piezoelectric actuator static characteristics.

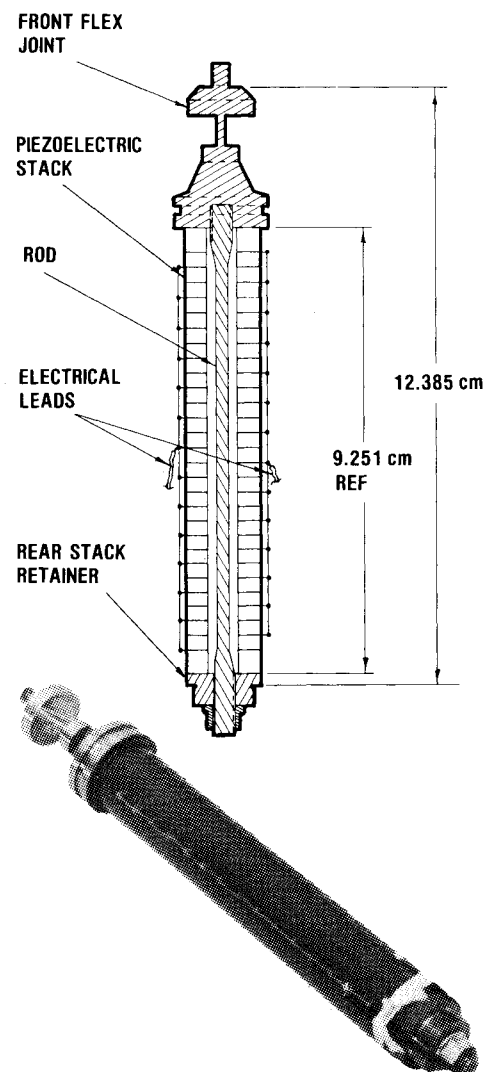


Fig. 4 Typical piezoelectric stack assembly.

Table 1 Actuator design example

Actuator length <sup>a</sup>	8.56 cm
Actuator stiffness	
End-to-end	35 N/μm (approx)
Active disks only	107 N/μm
Maximum free extension	12.6 μm
Maximum amplifier voltage	± 1500 V
Material <sup>b</sup>	Channel Industries 5400
Extension constant	$280 \times 10^{-12}$ m/V
Relative dielectric constant	1300
Number of active wafers	30
Wafer thickness <sup>a</sup>	0.301 cm
Wafer inner/outer diameter	0.635/1.588 cm
Capacitance	21.3 nf

<sup>a</sup> Active disk dielectric + electrode.<sup>b</sup> Equivalent to Clevite designation PZT4.

The purpose of the center rod is to apply a preload to the entire stack for mechanical and electrical stability. The purpose of the front flex joint is to permit mirror surface attachment without excessive transverse actuator loading.

Major design details for this design are given in Table 1. The tabulated length, which applies only to the 30 active disks plus electrodes, is naturally less than the length including isolating wafers and end fittings. The end-to-end stiffness is significantly less than that for the wafers alone. The amplifier output requirement of 1500 V is a major problem for amplifier solid-state output switching circuitry and insulation hardware design. As required, the same actuator extension can be obtained with a reduced output voltage if the number of actuator wafers is increased by the same factor. An alternate material to the one tabulated which would result in a similar design was Clevite PZT8 or the equivalent Channel 5800. Other actuator designs are discussed in Ref. 1.

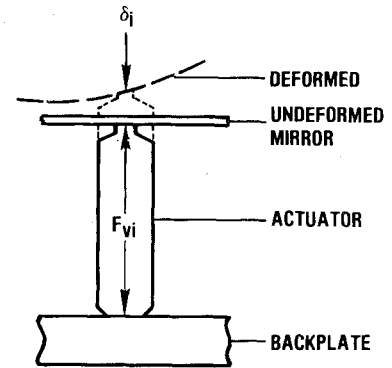
#### Actuator Drive Algorithm

Figure 5 illustrates the application of external equal and opposite forces at the actuator ends for the  $i$ th actuator ( $i = 1, \dots, N$ , where  $N$  is the total number of actuators). This array of external forces  $F_{vi}$ ,  $i = 1, \dots, N$  applied to the complete mirror-actuator backplate structural assembly causes an array of actuator and equal mirror longitudinal deformations  $\delta_i$ ,  $i = 1, \dots, N$ . As mentioned previously and repeated here for emphasis, the external force  $F_{vi}$  is the result of the voltage applied to the  $i$ th actuator terminals, which is the same as the blocked force.

The actuator algorithm is developed, using matrix notation, as seen in Fig. 5. The applied external force equals the assembly stiffness matrix multiplied by the deflection.  $\{F_v\}$  and  $\{\delta\}$  are  $1 \times N$  column matrices.  $\{K\}$  is the  $N \times N$  stiffness matrix whose elements  $K_{ij}$  are the structural influence coefficients for the complete mirror faceplate-actuators-backplate assembly specifically defined in Fig. 5. Replacing the actual deflection by the command deflection  $\{\delta_c\}$  and solving for the required actuator terminal voltage yields the desired mirror surface control actuator algorithm. As also illustrated in Fig. 5, implementation of the algorithm would consist of an assembly of  $N$  coefficient multipliers at the input of each amplifier.

As the relationship between the applied external force and the resultant deformation only applies below structural resonance frequencies, the actuator algorithm is identically limited.

A digital simulation was employed to verify the algorithm. A variety of surface contours was commanded and, as expected from the straightforward nature of the algorithm, the resultant actual contour was in agreement. An example result is shown in Fig. 6. To reduce input requirements, a quarter-section structural model was used. This modeling causes each external force and resultant deformation to be equal in each



$$\{F_v\} = \{K\} \{\delta\} \text{ where } K_{ij} \doteq \partial F_{vi} / \partial \delta_j$$

$$\{F_v\} = K_a n d_{33} \{V\}$$

$$\therefore \{V\} = \{K\} \{\delta_c\} / (K_a n d_{33}) \text{ with } \delta = \delta_c$$

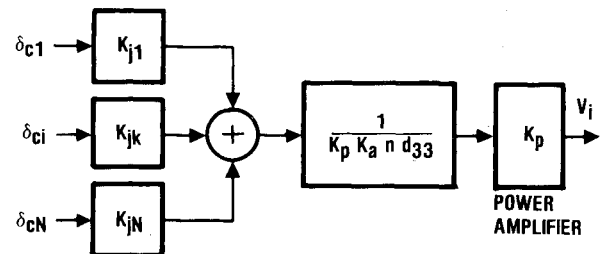


Fig. 5 Mirror surface control actuator/algorithm.

of four symmetric quarters of the total assembly. A maximum extension of actuator 329 with all others at zero was commanded. The required actuator voltage was determined and applied. Blocked and total force are also tabulated for reference. Note that the terminal voltage on the nonextending actuators is not zero and that pulling back on most of the adjacent actuators is required. High and low influence actuators are identified. The remainder are intermediate influence. One would intuitively expect that the low-influence actuators would be those furthest away from actuator 329, the high-influence actuators nearest, and the intermediate-influence actuators in between. The result obtained agrees fairly well with this expectation. The utility of this data is determination of how many input dividers (Fig. 5) are required to adequately compensate for mirror-faceplate coupling. In this respect, the four high-influence neighbors are clearly required and the four low-influence (remote located) actuators are not. The requirement for inclusion of the intermediate influence actuators depends upon accuracy requirements for the specific application.

To determine the bandpass capability, frequency responses for a variety of command surface contours were digitally calculated. Figure 7 is the frequency response for the command surface contour of Fig. 6. The fact that the transfer characteristic was unity at low frequency further verified the actuator surface control algorithm. More importantly, it was predicted that the mirror assembly backup structure was the bandpass-limiting element rather than the expected actuator resonance. Increasing the backplate stiffness resulted in the design configuration previously shown in Fig. 1.

The existence of such lightly damped resonances in the forward loop, in the neighborhood of 1 kHz, is not conducive to obtaining a 1 kHz closed-loop bandpass. Adding a rolloff filter probably would not be successful because the resonances are too large and close to the desired 1 kHz bandpass. Another approach, one which the authors understand has already been successfully used by others, is to damp the resonances by using the voltage output from an added electrically insulated sensing wafer in the piezoelectric stack.

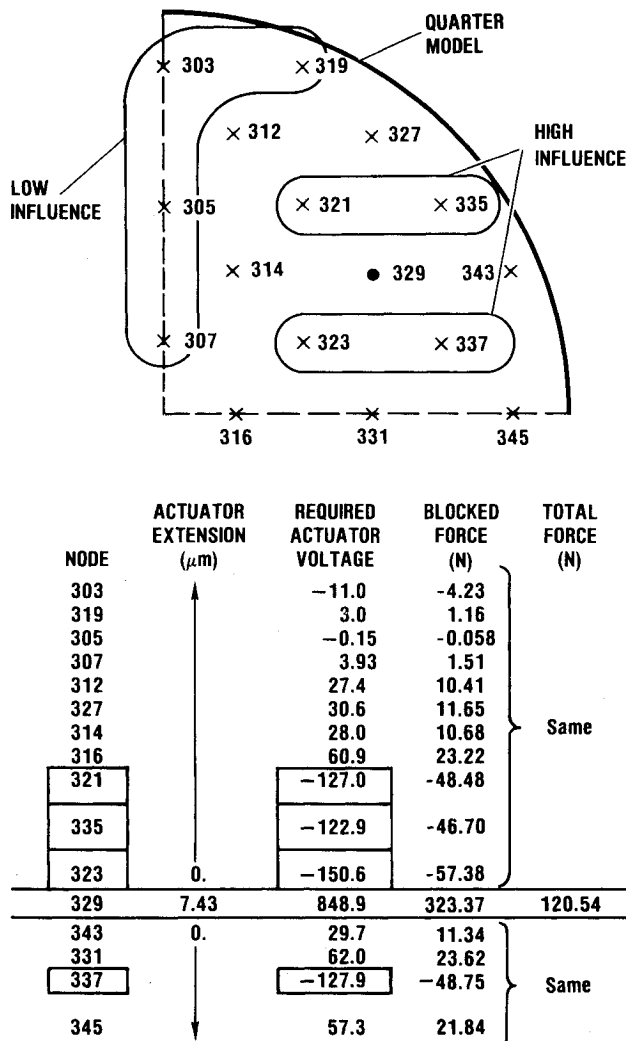


Fig. 6 Actuator algorithm test (static).

### Actuator Drive Amplifier

The hardware approach selected is a solid-state switching amplifier. It arose from prior developments in high-fidelity audio systems and sonar transducer amplifiers.<sup>5,6</sup> Relative to these past efforts, the piezoelectric actuator unique requirements were high voltage and capacitive load. The major performance feature sought is transfer of energy from the power supply to the capacitive load with minimum power loss integral to the amplifier.

Figure 8 shows the overall configuration, an equivalent simplified output circuit, and basic operational waveforms. The amplifier "H" or full-wave bridge output configuration was selected because it provided plus and minus outputs using a single-ended power supply and it nominally halved the output transistor back-voltage requirement due to the series connection of two switching transistors in the charge path. The modulator or control element closes and opens a dc power source into the piezoelectric capacitive load. The series inductor limits the charge-discharge current into the load to incrementally change the voltage output. While this amplifier includes several novel features, one of which is patented, the element of primary concern herein is the modulator.

### Amplifier Operation

The waveforms shown in Fig. 8 correspond to the special case where the output voltage  $V_c$  equals zero. Later the analysis is extended to include the case where the output voltage is anywhere between its plus and minus output limits.

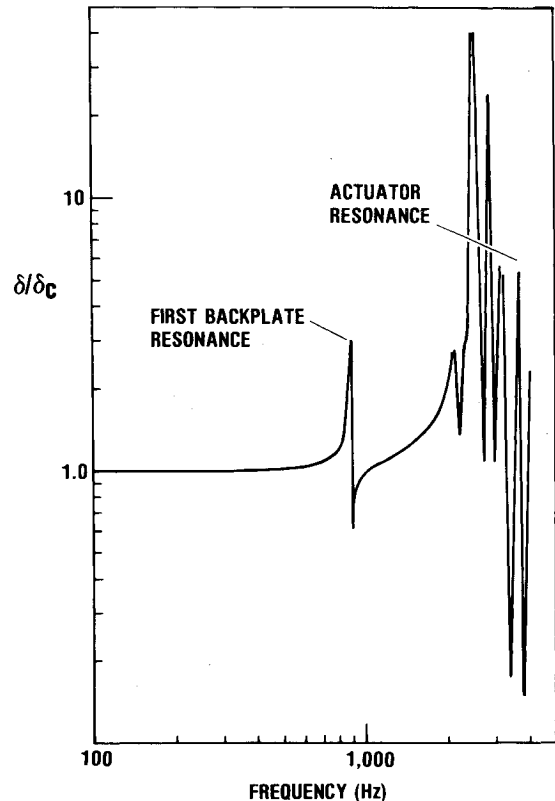


Fig. 7 Calculated actuator-assembly bandpass (node 329).

For the simplified output circuit, the wiring and load ground connection is different from the actual "H" configuration used. However, essential operation and waveforms are identical and more easily understood. Assume that the plus charge switch is closed for a time  $t_0$ , thereby applying a voltage  $V_i$  equal to the supply voltage  $E$  across the series inductor  $L$  and load capacitor  $C$ . The inductor provides a smooth current ( $I$ ) rise upon charge switch closure and opening. Without it, theoretically infinite current would be drawn through the charge switch. The charge switch is opened when the output voltage has increased to half the desired quantization level,  $\Delta V_{c0}$ . At this time, the charge current has reached its maximum level of  $I_{p0}$ . Current within the inductor attempting to decrease through the high back-resistance of the charge switches causes the voltage  $V_i$  to instantly attempt to fall to a value well below the negative supply voltage  $E$ . This fall is stopped at the  $-E$  value by the "clamping" diode connected to the  $-E$  supply which now provides a path for the inductor current to flow back into the  $-E$  supply. The direction of the current is such to recharge the supply. During this phase  $V_i$  is  $-E$ , causing the current to reduce from the peak value  $I_{p0}$  at the same rate as it rose. This current reduction continues until the current is zero, at which time the output voltage has changed in an amount equal to the quantization level  $\Delta V_{c0}$ . After the current has reached zero, if there is a demand for further change in output voltage, the operation is repeated. Otherwise, it is not repeated and the load capacitor remains charged at its new output level. There is a tendency for the capacitor to discharge through its own leakage resistance and the back impedance of the charge switches, but the rate is extremely low because the resistances are of the order of a megohm. The time  $t_0$  is short in comparison to the LC circuit oscillation period, so the current rise and fall is essentially at constant rate.

### Output Circuit Design

Table 2 lists input requirements pertinent to this amplifier design and derived major output circuit design relations.

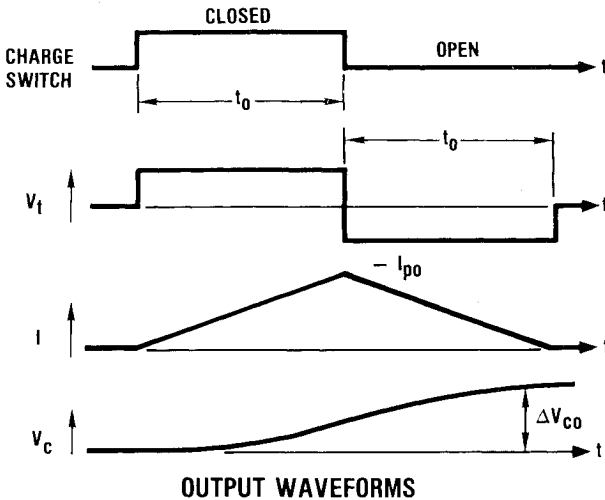
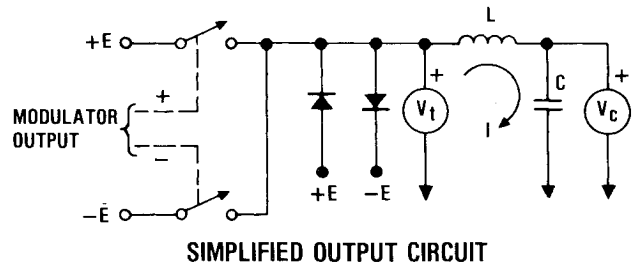
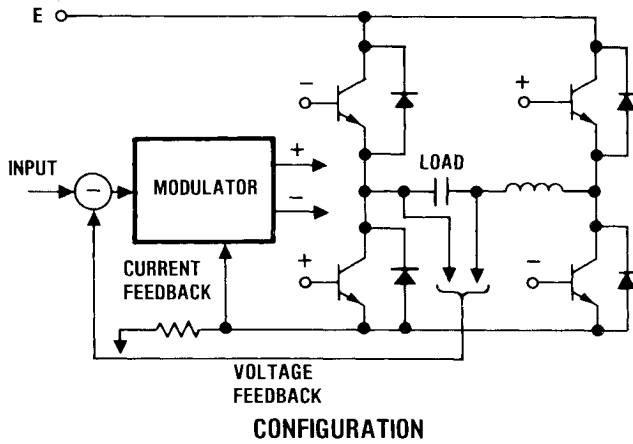


Fig. 8 Amplifier configuration and operation.

Example input-output values are also given. The maximum output requirement is limited by available output switching transistors. The output quantization is the minimum amount of output voltage change that is determined by the control resolution requirement. Assuming that the mirror is moved one wavelength,  $\lambda$ , upon application of 1500 V, a 30-V quantization level corresponds to a  $\lambda/50$  control resolution which was adequate in this application. Quantization level is also the amplifier output noise. The maximum slew rate or output voltage time derivative is equivalent to amplifier bandpass. For example, it corresponds to a sinusoidal output of 3000 V peak-to-peak at 400 Hz. The load capacity is, of course, that of the piezoelectric actuator.

The basic capacitor and inductor design relations are

$$V_t - V_c = LI \quad \Delta V_c = \frac{1}{C} \int_0^t Idt \quad (1)$$

Table 2 Determination of output circuit requirements

Input requirements:	Example value
Maximum output voltage, $V_{cm}$	1500 V
Output quantization, $\Delta V_{c0}$	30 V
Maximum slew rate, $\dot{V}_{cm} = \omega_c V_{cm}^a$	3.7 V/ $\mu$ s
Load capacitance, $C$	50 nF
Derived output circuit requirements ( $V_c = 0$ ):	
Switch on-time, $t_0 = \Delta V_{c0} / (2 \dot{V}_{cm})$	3.98 $\mu$ s
Peak current, $I_{p0} = 2 \dot{V}_{cm} C$	0.38 A
Inductance, $L = \Delta V_{c0} E / (4 \dot{V}_{cm}^2 C)^b$	15.83 mH

<sup>a</sup>  $\omega_c = 2\pi 400$  rad/s.

<sup>b</sup>  $E = V_{cm}$ .

Using the assumptions of  $V_c = 0$  and a constant current rise and fall rate of  $K$  A/s (illustrated in Fig. 8) yields

$$E = LI \dot{I} = \begin{cases} K & (0 \leq t \leq t_0) \\ -K & (t_0 \leq t \leq 2t_0) \end{cases} \quad (2)$$

$$\Delta V_{c0} = \frac{2}{C} \int_0^{t_0} Idt \quad \dot{V}_{cm} = \Delta V_{c0} / (2t_0) \quad (3)$$

Algebraic manipulation of Eqs. (2) and (3) yields the derived output circuit relations of Table 2. These, together with the maximum output voltage, are needed to select or design the output transistor switches and the series inductor.

#### Modulator Development

Pulse width modulation (PWM) is used. Specifically, the charge time period is varied from  $t_0$  to compensate for the output  $V_c$  being anywhere within  $\pm E$ . This is very important because the charging current rate is proportional to the difference between  $E$  and  $V_c$ . Alternate methods of PWM were studied. Criteria for selection are slew rate capability, equivalent to speed of response, and output quantization, equivalent to noise.

Figure 9 is a PWM example illustrating variation of the charge time  $t_i$  to produce a constant voltage increment ( $\Delta V_c = \Delta V_{c0}$ ) per charge period independent of  $V_c$ . In Fig. 9, and following figures, the quantity  $R$  is the ratio of the output voltage  $V_c$  to the constant supply voltage magnitude  $E$ . As  $V_c$  varies between plus and minus  $E$ ,  $R$  varies between plus and minus one. With  $R$  equal to minus one,  $V_c$  equals minus  $E$ ; should the plus  $E$  modulator output switch be closed (see Fig. 8), the current rise rate would be a maximum due to the existence of  $2E$  V across the inductor. The charge flow would be in a direction to change the output voltage  $V_c$  from its maximum negative value to a more positive value. In this situation, a minimum charge time  $t_i$  would be required to change the output voltage  $V_c$  in an amount  $\Delta V_{c0}$ . This is the situation illustrated in Fig. 9 for negative  $R$ . As  $R$  increases, the charge time  $t_i$  requirement increases. For  $R$  at zero,  $t_i$  is increased to  $t_0$  and for  $R$  positive,  $t_i$  increases further. Note that as  $R$  approaches zero from either polarity, the peak charging current increases toward  $I_{p0}$  and the total charge-discharge time decreases. As controlled by the modulator, the total effect is to cause an equal area under the current vs time pulse, which corresponds to an equal voltage increment independent of the value of  $R$ .

Table 3 identifies three applicable PWM techniques together with their basic constraint, and gives relations for the slew rate and quantization selection criteria. The cutoff voltage, also shown, is a basic PWM mechanization formula as it corresponds to the output voltage rise during the charge time interval (see Fig. 9). The relations are based on use of Eq.

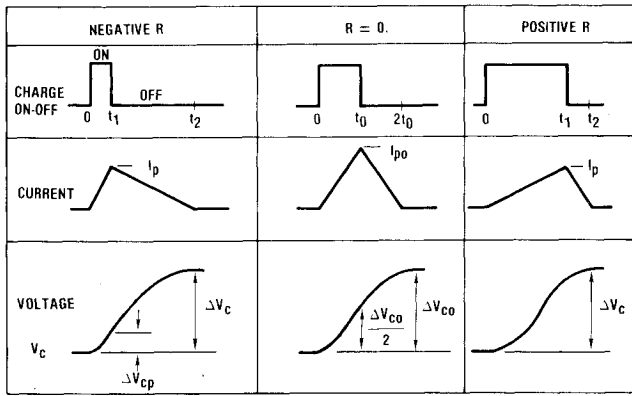


Fig. 9 Example PWM compensation for output voltage state (constant quantization).

(1) and the assumption that the current time derivative is constant during the current rise and fall periods. The absolute value of the constant, however, is now different for the two periods. The relations apply for a positive polarity change in output voltage. For a negative polarity change, some of the relations exhibit a change in sign.

Figure 10 is a plot of the selection criteria as a function of output voltage to supply voltage ratio  $R$ . The selection criteria are normalized to the value at zero output voltage where all modulation methods have identical performance. The performance changes significantly at high output voltage, as shown in Fig. 10. The slew rate or bandpass capability of constant slew rate modulation is highest, constant quantization is intermediate, and fixed frequency is least. With respect to quantization or noise output, the situation reverses. For fixed frequency, the noise reduces as output voltage increases. Constant quantization modulation exhibits a flat noise characteristic. Constant slew rate modulation exhibits a high noise potential.

The present selection is constant quantization because of its intermediate position with respect to bandpass and noise performance characteristics. This selection would change depending upon specific requirements. If noise relative to bandpass requirements were severe, the constant frequency method would be appropriate. For a reverse weighing of requirements, constant slew rate would be appropriate. A further comment with respect to noise is that fixed frequency currently has the best potential for improvement via an output filter.

Figure 11 illustrates the variable hysteresis-type logic required to implement the selected PWM constant quantization technique. The error voltage input  $V_e$  is the difference between amplifier input and output voltage with a gain of unity. Routine scaling accommodates any other amplifier gain. Mechanization is by electronic analog circuitry. As shown, a corrective charge is initiated whenever the error voltage magnitude exceeds the fixed, preselected value of  $\Delta V_{co}$ . This corrective charge is terminated after a time  $t_i$  (see

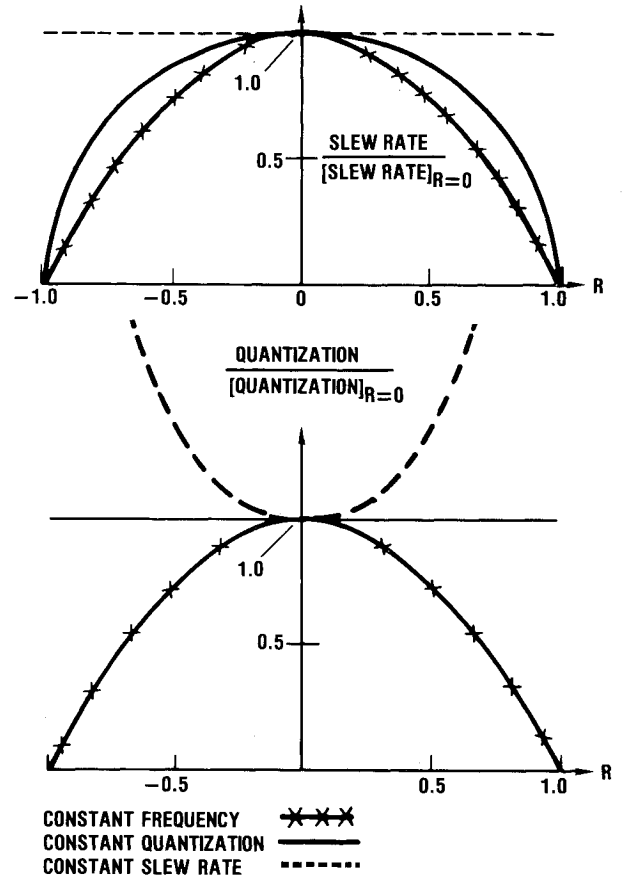


Fig. 10 Performance comparison of alternate PWM methods.

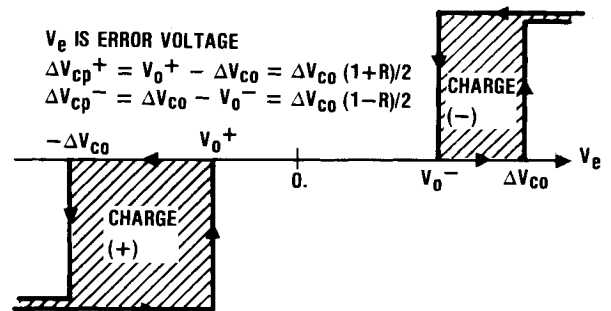


Fig. 11 Threshold logic for constant quantization PWM.

Fig. 9) as sensed by a change in corrective voltage equal to either  $\Delta V_{cp}^-$  or  $\Delta V_{cp}^+$ , depending on the error polarity. This  $\Delta V_{cp}^-$  relationship was developed previously in Table 3. The  $\Delta V_{cp}^-$  relationship is similarly obtained with polarity considered. The mechanization of charge termination uses the voltages  $V_0^+$  and  $V_0^-$ , which are obtained directly from the two rightmost relations on Fig. 11.

Table 3 Definition of alternate PWM methods

Modulation technique	Constraint	Slew rate ( $I_p/I_{p0}$ )	Quantization ( $\Delta V_c/\Delta V_{co}$ )	Cutoff voltage ( $\Delta V_{cp}/\Delta V_{co}$ )
Constant frequency	$t_2 = 2t_0$	$(1-R)^{2a}$	$(1-R)^2$	$(1+R)^2(1-R)/2$
Constant quantization	$\Delta V_c = \Delta V_{co}$	$(1-R^2)^{1/2}$	1.0	$(1+R)/2$
Constant slew rate	$I_p = I_{p0}$	1.0	$(1-R^2)^{-1}$	$1/[2(1-R)]$

<sup>a</sup>  $R = V_c/E$  and equations are for increasing  $V_c$ .

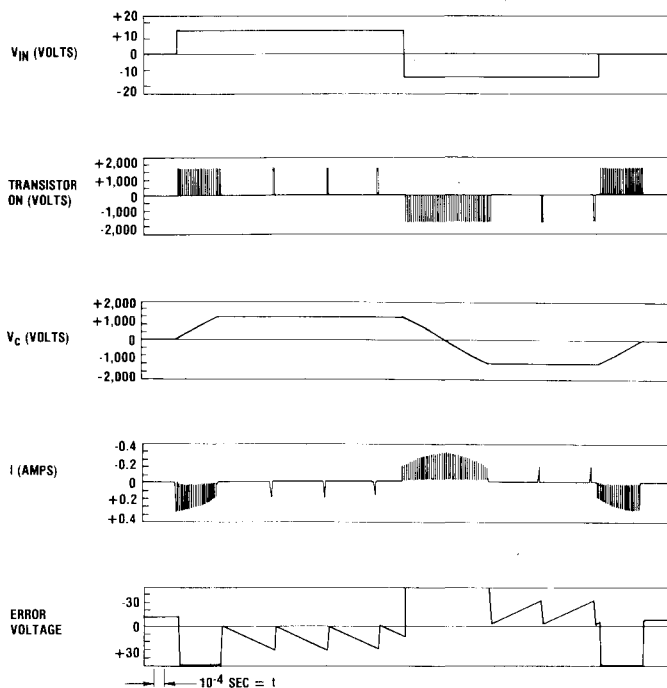


Fig. 12 Analog computer simulation verification of PWM approach (PWM example).

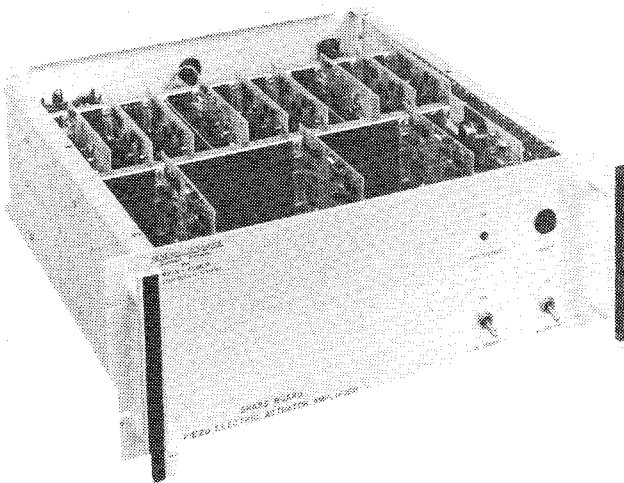


Fig. 13 Brassboard of a three-channel piezoelectric actuator amplifier.

Current limiting is also required to protect the output circuitry. For example, assume an initial state of zero volts input and output with a subsequent step input voltage calling for a maximum positive output. The error voltage is instantly  $-1500$  V, causing the positive charge switch to close. If one relied completely upon the variable threshold logic, the current would rise to well above that required to yield the required voltage slew rate. To prevent this excess current, the charge is also terminated when the current exceeds the peak value  $I_{po}$ . Should the charge switch be opened by the current limit, it is retained in the open position until the current has dropped to zero, after which it is closed again to repeat the cycle. An alternate and perhaps more descriptive explanation of this recommended control is that constant slew rate is employed whenever the amplifier is in an overdriven condition. However, when driven within slew rate limits, constant quantization is employed.

Table 4 Brassboard amplifier design data

Specifications:

Input voltage	$\pm 10$ V
Maximum output	$\pm 1400$ V peak
Output quantization	3.5 V
Maximum slew rate	$0.126$ V/ $\mu$ S
Power supply	1500 V
Load	$0.5$ $\mu$ f

Performance:

Maximum loss	5 W <sup>a</sup>
Power supply rejection	> 40 dB
Common mode rejection	> 40 dB
Distortion	< 1% at 700 V out
Linearity	$\pm 1\%$

<sup>a</sup> At maximum reactive power output of 62 VA.

### Analog Simulation

Modulator design was verified by simulating the output circuit, inductor-capacitive load, and modulator on an analog computer. Component imperfections such as transistor switch forward and back resistance, inductor series resistance, and piezoelectric actuator leakage resistance were included. Figure 12 shows a sample output computer trace for the constant quantization modulator approach. For this run, the modulator implemented the constant slew rate current control. The output circuit design corresponded to that of Table 2. A step  $\pm 10$  V input was applied. The amplifier gain was 150 V/V and maximum output voltage was 1500 V. The output voltage feedback was appropriately scaled down by the amplifier gain of 150 to form the error input. The charge current pulses amplitude appropriately varied with output voltage buildup to the maximum. Further note that only a few current impulses are required to hold output voltage which decays slightly due to the load capacitor leakage resistance and the back resistance of the output switching transistors. The error voltage was consistently controlled within  $\pm 30$  V threshold limits except those times when the input was step-changed.

### Hardware Example

A number of amplifiers have been designed and built based on the principles discussed in this paper. Figure 13 is a photograph of a three-channel amplifier used with a three-actuator focus control mirror. The relationships in Table 4 were used to design the output circuit. Load series inductance was 94 mH, and the peak load current required was 0.19 A. Reference 3 provides a detailed description of this amplifier.

Note that losses of only 5 W were incurred in delivering 62 V-A (rms) into the piezoelectric actuator capacitive load. The maximum output rating was slightly reduced from 1500 V to 1400 V for transistor reverse voltage limitation reasons.

### Conclusions

- 1) An actuation control algorithm for focus control by mirror surface deformation has been developed and analytically verified.
- 2) The ability of piezoelectric actuators to provide high bandpass (1 kHz) and from 1 to 10  $\mu$ m surface deformations has been shown. The requirement for a high-voltage output drive amplifier for a capacitive load was satisfied.
- 3) A unique solid-state amplifier design appropriate to driving the piezoelectric actuator is available.
- 4) Hardware design examples for the actuator and amplifier are shown.

### Acknowledgments

The authors wish to thank R.E. Zammit for the significant contributions he made to the development of the analog computer simulation and amplifier hardware.

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